

SEMICONDUCTOR MEMORY DEVICE

INCLUDING PAGE LATCH CIRCUIT

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of U.S. Application No. 09/794,076, filed February 28, 2001, the entire contents of which are incorporated herein by reference.

[0002] This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No.2000-066954, filed March 10, 2000, the entire contents of which are incorporated herein by reference.

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BACKGROUND OF THE INVENTION

[0003] 1. Field of the Invention

[0004] This present invention relates to a semiconductor memory device which is reprogrammable, and particularly relates to a reprogrammable semiconductor memory device having a page latch.

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[0005] 2. Related Art

[0006] In some of a nonvolatile semiconductor memory device (EEPROM) which is reprogrammable by one byte to by a few tens bytes (for one page), one latch circuit (page latch circuit) for retaining one page data is provided for every bit line. In this specification, the nonvolatile semiconductor memory device is called a semiconductor memory device having a page latch.

[0007] An operation of a conventional nonvolatile semiconductor memory device having a page latch will be explained. Figs. 18a to 18c indicate data flow diagrams at a data loading operation, at a programming operation and at a read operation in a conventional semiconductor memory device having a page latch, respectively. First of all, as shown in Fig. 18a, one-page program data are loaded to a page latch. When one-page program data are stored in the page latch, typically one page data stored in memory cells are erased.

[0008] As shown in Fig. 18b, the one-page program data in the page latch are simultaneously written to the one-page memory cells, whose previous data have been erased. Also, when a data in the memory cell is read out, as shown in Fig. 18c, a selected memory cell is connected to a read out circuit and the data is read from the selected memory cell.

[0009] However, once a data loading operation is started, the operation continues to a data erasing operation and a data programming operation automatically in the conventional nonvolatile semiconductor memory device with a page lath. Also, in the data reading out operation, the conventional nonvolatile semiconductor memory device only has a mode in which the operation reads out data programmed to the memory cell.

[00010] In such conventional nonvolatile memory devices with page latches, when a data is programmed to a memory cell and the programmed data is read out from the memory cell, and assuming that the data which is read out includes an error, it is very hard to determine whether the data which is programmed to the memory cell has included the error or the data which is read out from the memory cell was broken at the read out circuit.

[00011] Also, when you test the page latch and the read out circuit in the conventional nonvolatile semiconductor memory device, you need a very long time to test because a data is programmed to a memory cell automatically.

SUMMARY OF THE INVENTION

[00012] An object of this invention is to provide a semiconductor memory device capable of making it easy to determine a cause of an error if there is an error in reprogrammed data and carrying out a test of the page latches and the read out circuits in a short time.

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[00013] In order to accomplish the above object of this invention, a semiconductor memory device related to this invention comprises a bit line to which a reprogrammable memory cell is connected, a data bus on which data is transferred, a latch circuit having latching the data transferred on the data bus, a read out circuit connected to the data bus and a data transfer circuit group has an ability to directly transfer the data latched in the latch circuit, to the read out circuit without via the memory cell.

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[00014] The data transfer circuit may have a first operation mode to transfer a data loaded to the latch circuit, to the memory cell connected to the bit line, a second operation mode to a data read out from the memory cell to the read circuit and a third operation mode to directly transfer the data latched in the latch circuit, to the read circuit.

[00015] The third operation mode may be performed during a test of the semiconductor memory device.

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[00016] The first and the second operation mode may be performed during a normal operation and the third operation mode is performed during a test of the semiconductor memory device.

[00017] The data transfer circuit group may have a first transfer gate, an one end of which electrically connected to the bit line, a second transfer gate, an one end of which electrically connected to an other end of the first transfer gate, a third transfer gate, an one end of which electrically connected to the one end of the first transfer gate and an other end

of which electrically connected to the latch circuit and a fourth transfer gate, an one end of which electrically connected to an other end of the second transfer gate and an other end of which electrically connected to the read out circuit.

[00018] It is desirable that when a data loaded to the latch circuit is transferred to the memory cell, the first transfer gate is set to ON state, the second transfer gate is set to OFF state, the third transfer gate is set to ON state, the fourth transfer gate is set to ON state, when a data read out from the memory cell is transferred to the read out circuit, the first transfer gate is set to ON state, the second transfer gate is set to ON state, the third transfer gate is set to OFF state, the fourth transfer gate is set to ON state, when a data loaded to the latch circuit is directly transferred to the read out circuit without via the memory cell, the first transfer gate is set to OFF state, the second transfer gate is set to ON state, the third transfer gate is set to ON state, the fourth transfer gate is set to ON state.

[00019] A voltage of a gate electrode of the third transfer gate may be gradually raised to set to ON state.

[00020] It may be desirable that when a data loaded to the latch circuit is transferred to the memory cell, the first transfer gate is set to ON state, the second transfer gate is set to OFF state, the third transfer gate is set to ON state, the fourth transfer gate is set to OFF state, when a data read out from the memory cell is transferred to the read out circuit, the first transfer gate is set to ON state, the second transfer gate is set to ON state, the third transfer gate is set to OFF state, the fourth transfer gate is set to ON state, when a data loaded to the latch circuit is transferred to the read out circuit, the first to the fourth transfer gate are set to ON state, the memory cell is set to non-selected state.

[00021] A voltage of a gate electrode of the third transfer gate may be gradually raised to set to ON state.

[00022] The semiconductor memory device having a data latch circuit further comprises a control circuit controlling the transfer gate group so as to achieve a first and second operation modes, the first operation mode programming a data loaded to the latch circuit, to the memory cell, the second operation mode stopping an operation after a data is loaded to the latch circuit.

[00023] The first operation mode may be performed at a normal operation, the second operation mode is performed at a testing operation.

[00024] The semiconductor memory device having a data latch circuit further comprises an error correction circuit is electrically connected to the read out circuit.

[00025] A semiconductor memory device having a data latch circuit comprise, a bit line to which a reprogrammable memory cell is connected, a data bus on which data is transferred, a latch circuit having latching the data transferred on the data bus, a read out circuit connected to the data bus and a data transfer circuit group, wherein the data transfer circuit group is controlled so as to transfer the data latched in the latch circuit, to the read out circuit without via the memory cell.

[00026] The data transfer circuit may have a first operation mode to transfer a data loaded to the latch circuit, to the memory cell connected to the bit line, a second operation mode to a data read out from the memory cell to the read circuit and a third operation mode to directly transfer the data latched in the latch circuit, to the read circuit.

[00027] The third operation mode may be performed during a test of the semiconductor memory device.

[00028] The first and the second operation mode may be performed during a normal operation and the third operation mode may be performed during a test of the semiconductor memory device.

[00029] It is desirable that the data transfer circuit group has a first transfer gate, an one end of which electrically connected to the bit line, a second transfer gate, an one end of which electrically connected to an other end of the first transfer gate, a third transfer gate, an one end of which electrically connected to the one end of the first transfer gate and an other end of which electrically connected to the latch circuit and a fourth transfer gate, an one end of which electrically connected to an other end of the second transfer gate and an other end of which electrically connected to the read out circuit.

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[00030] It is desirable that when a data loaded to the latch circuit is transferred to the memory cell, the first transfer gate is set to ON state, the second transfer gate is set to OFF state, the third transfer gate is set to ON state, the fourth transfer gate is set to ON state, when a data read out from the memory cell is transferred to the read out circuit, the first transfer gate is set to ON state, the second transfer gate is set to ON state, the third transfer gate is set to OFF state, the fourth transfer gate is set to ON state, when a data loaded to the latch circuit is directly transferred to the read out circuit without via the memory cell, the first transfer gate is set to OFF state, the second transfer gate is set to ON state, the third transfer gate is set to ON state, the fourth transfer gate is set to ON state.

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[00031] A voltage of a gate electrode of the third transfer gate may be gradually raised to set to ON state.

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[00032] It may be desirable that when a data loaded to the latch circuit is transferred to the memory cell, the first transfer gate is set to ON state, the second transfer gate is set to OFF state, the third transfer gate is set to ON state, the fourth transfer gate is set to OFF state, when a data read out from the memory cell is transferred to the read out circuit, the first transfer gate is set to ON state, the second transfer gate is set to ON state, the third transfer gate is set to OFF state, the fourth transfer gate is set to ON state, when a data loaded to the

latch circuit is transferred to the read out circuit, the first to the fourth transfer gate are set to ON state, the memory cell is set to non-selected state.

[00033] A voltage of a gate electrode of the third transfer gate may be gradually raised to set to ON state.

5 [00034] The semiconductor memory device having a data latch circuit further comprises a control circuit controlling the transfer gate group so as to achieve a first and second operation modes, the first operation mode programming a data loaded to the latch circuit, to the memory cell, the second operation mode stopping an operation after a data is loaded to the latch circuit.

10 [00035] The first operation mode may be performed at a normal operation, the second operation mode is performed at a testing operation.

[00036] The semiconductor memory device having a data latch circuit further comprises an error correction circuit is electrically connected to the read out circuit.

15 [00037] A test method of a semiconductor memory device comprises steps of; latching data at a page latch via a data bus on which the data are transferred, transferring the data latched in the page latch to a cell matrix for stored the data at a first mode and to a read out circuit at a second mode for testing whether or not an error occurs at a data transfer circuit group including the data bus, the page latch and read out circuit.

20 BRIEF DESCRIPTION OF THE DRAWINGS

[00038] Fig. 1a and Fig. 1b show data flows respectively in a case that a semiconductor memory device of a first embodiment of this invention is set for a data loading operation and a page latch reading out operation.

[00039] Fig. 2 shows a circuit example of a page latch which is provided in the semiconductor memory device of the first embodiment of this invention.

[00040] Fig. 3 shows a waveform diagram which indicates a data loading operation of the page latch in Fig. 2.

5 [00041] Fig. 4 shows a waveform diagram which indicates a programming operation of the page latch in Fig. 2.

[00042] Fig. 5 shows a waveform diagram which indicates a reading out operation of the page latch in Fig. 2.

10 [00043] Fig. 6 shows a waveform diagram which indicates a page latch reading out operation of the page latch in Fig. 2.

[00044] Fig. 7a shows a state of the page latch at a data loading operation. Fig. 7b shows a state of the page latch at a programming operation. Fig. 7c shows a state of the page latch at reading out operation. Fig. 7d shows a state of the page latch at a page latch reading out operation.

15 [00045] Fig. 8a and Fig. 8b show a circuit diagram of a control circuit to control a transfer signal N2.

[00046] Fig. 9 shows a waveform diagram which indicates another page latch reading out operation of a page latch in Fig. 2.

20 [00047] Fig. 10a shows a circuit diagram of a NOR type nonvolatile semiconductor memory device. Fig. 10b shows a circuit diagram of a three-transistor type nonvolatile semiconductor memory device.

[00048] Fig. 11 shows a block diagram of one example of the control circuit.

[00049] Fig. 12 shows a waveform diagram, which indicates a normal operation of the control circuit in Fig. 11.

[00050] Fig. 13 shows a waveform diagram which indicates a normal operation of the control circuit in Fig. 11.

[00051] Fig. 14 shows a waveform diagram which indicates a testing operation of the control circuit in Fig. 11.

5 [00052] Fig. 15 shows a flow chart which indicates a control sequence of the control circuit.

[00053] Fig. 16a and Fig. 16b show data flows respectively in a case that a semiconductor memory device of a second embodiment of this invention is set for a data loading operation and a page latch reading out operation.

10 [00054] Fig. 17a to Fig. 17c show data flows at the data loading operation and the page latch reading out operation of the second embodiment of this invention respectively.

[00055] Fig. 18a to Fig. 18c show data flows at the data loading operation, the data programming operation and the data reading out operation of the conventional semiconductor memory device respectively.

15 [00056] Figs. 19 and 20 show examples of a memory card.

[00057] Fig. 21 shows an example of a card holder.

[00058] Figs. 22 and 23 show examples of application of the invention

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

20 [00059] Embodiments of the invention are explained with reference to figures, in which same numbers refer to same parts throughout the figures.

[00060] FIRST EMBODIMENT.

[00061] Fig. 1a and 1b show data flows at a data loading operation and at a data reading out operation from a page latch (page latch read) of a nonvolatile semiconductor memory device of a first embodiment, respectively. As shown in Fig. 1a, one page data are loaded to a page latch 11 via a data bus 1 at the data loading operation. Then, the conventional nonvolatile semiconductor memory device, erasing of data programmed in a memory cell and programming of the loaded data follow the loading operation continuously and automatically when program data of one page are set to the page latch 11.

[00062] On the other hand, in the nonvolatile semiconductor memory device of the first embodiment of this invention, the loading operation is once stopped when program data of one page are set to the page latch 11.

[00063] After the stop of the operation, as shown in Fig. 1b, the page latch 11 is electrically separated from a cell matrix 2 and, furthermore, is electrically connected to a read out circuit 27. Thereby, the data loaded to the page latch 11 can be transferred to the read out circuit 27 directly and read out from the page latch 11 without transferring the data to the cell matrix 2.

[00064] The reading out operation, which reads out the data from the page latch 11, for instance, is carried out at a testing operation. The reading out operation can be used for an examination for separating non-defect productions from defect productions and for a defect analysis of nonvolatile semiconductor memory device, or the like.

[00065] The nonvolatile semiconductor memory device of the first embodiment in this present invention can carry out operations shown in Fig. 18a to Fig. 18c at a normal operation. In other words, the nonvolatile semiconductor memory device of the first

embodiment in this present invention can be used, similarly to the conventional nonvolatile semiconductor memory device at the normal mode.

[00066] Next, one circuit example of the page latch 11 is described. Fig. 2 shows an exemplary circuit diagram of the page latch 11 contained in the nonvolatile semiconductor memory device of the first embodiment.

[00067] As shown in Fig. 2, the page latch 11 has first transfer gates 13-1 to 13-N, second transfer gates 15-1 to 15-N, third transfer gates 17-1 to 17-N and latch circuits 19-1 to 19-N, respectively. The first to third transfer gates comprise, for instance, MOS transistors.

[00068] Each one end of current paths of the fist transfer gates 13-1 to 13-N is connected to corresponding bit lines BL1 to BLN respectively. A transfer signal N3 is commonly supplied to control nodes of the first transfer gate 13-1 to 13-N.

[00069] Each one end of current paths of the second transfer gates 15-1 to 15-N is connected to corresponding ends of the current paths of the first transfer gates 13-1 to 13-N respectively, which are connected to a data line 21. The data line 21 is one line of the data bus 1 shown in Fig.1a and 1b. The data line 21 is connected to the read out circuit 27 via a fourth transfer gate 25. A transfer signal N4 is supplied to a control node of the fourth transfer gate 25. Select transfer signals N1[1] to N1[N] are supplied to the control nodes of the second transfer gates 15-1 to 15-N respectively. The select transfer signals N1[1] to N1[N] are column select signals and outputted from a decoder 3 (a column decoder) shown in Fig. 1a and Fig. 1b.

[00070] Each one end of current paths of the third transfer gates 17-1 to 17-N is connected to corresponding nodes 23-1 to 23-N respectively. Each of the nodes 23-1 to 23-N is the corresponding connection-node between the first transfer gates 13-1 to 13-N and the second transfer gates 15-1 to 15-N respectively. Each another end of current paths of the

third transfer gates 17-1 to 17-N is connected to corresponding latch circuits 19-1 to 19-N respectively. A transfer signal N2 is supplied to the control nodes of the third transfer gates 17-1 to 17-N commonly.

[00071] In the above-stated circuit, each gate of the first transfer gates 13-1 to 13-N, 5 the second transfer gates 15-1 to 15-N, the third transfer gates 17-1 to 17-N and the fourth transfer gates 25 functions as a data transfer circuit for transferring data. The data transfer circuit transfers data inputted on the data line 21 to the memory cell via the latch circuits 19-1 to 19-N and the bit lines BL1 to BLN, or transfers data via the data line 21 to the read out circuit 27.

[00072] In the page latch 11 shown in Fig. 2 the N latch circuits 19-1 to 19-N are 10 electrically connected to one data line 21. Therefore, at the data loading, data are loaded to the page latch 11 N times. When a total of N data are latched to the latch circuits 19-1 to 19-N, respectively, one page data are set to the page latch 19. After that, as shown in Fig. 1b, the page latch reading out operation or the data erasing and the data programming operations 15 are carried out.

[00073] The number of the latch circuits 19-1 to 19-N provided in the page latch 11 shown in Fig. 2 may be M (an integral number) in an actual device. In this case, parallel data 20 $M \times N$ (M parallel data, N times) are loaded to the M page latches 11 via the M data lines 21. When a total of $M \times N$ data are latched to the corresponding $M \times N$ latch circuits respectively, one page data is set in the page latches 11. After that, as shown in Fig. 1b, the page latch reading out operation, or the data erasing and the data programming operations are carried 25 out. Next, an example of operation of page latch 11 (Fig. 2) is described.

[00074] DATA LOADING OPERATION.

[00075] Fig. 3 shows waveform diagram s at the data loading operation of the data latch 11 shown in Fig. 2. Also, Fig. 7a shows states of the page latch 11 at the data loading operation.

[00076] As shown in Fig. 3, at a time t1, a chip enable signal /CE and a write enable signal /WE are set from High level to Low level respectively. When each of the chip enable signal /CE and the write enable signal /WE is set to Low level, the transfer signals N3 and N4 are set from High level to Low level respectively.

[00077] As a result, the first transfer gates 13-1 to 13-N and the fourth transfer gate 25 are set to OFF respectively, the page latch 11 is electrically separated from the cell matrix 2 and the read out circuit 27. When the chip enable signal /CE and the write enable signal /WE are set to Low level, an address signal ADD is inputted to the chip. As a result, typically one of the N select transfer signals N1[1] to N1[N] is selected in accordance with the inputted address signal ADD, and the selected signal (for example, the select transfer gate signal N1[1]) is set from Low level to High level. This causes the second transfer gate 15-1 to turn ON, and the data DATA is transferred from the data line 21 to the connection node 23-1.

[00078] Next, at a time t2, a transfer signal N2 is set to High level, thereby forcing the third transfer gates 17-1 to 17-N to turn ON respectively. As a result, as shown in Fig. 7a, the data DATA is transferred to the latch circuit 19-1 from the data line 21 via the connection node 23-1, and latched by the latch circuit 19-1.

[00079] Same operations are repeated from times t3 to t8. Thereby, the data DATA are transferred to all of the latch circuits 19-1 to 19-N and the N data are latched to the corresponding latch circuits 19-1 to 19-N respectively. And at a time t9, a DATA LOAD END signal is set to High level contemporarily, thereby finishing the data loading operation.

[00080] PROGRAMMING OPERATION.

[00081] The programming operation is carried out after the erasing operation. Fig. 4 shows waveform diagrams of the programming operation of the page latch 11 illustrated in Fig. 2. Fig. 7a shows a diagram illustrating a state of the page latch 11 at the programming operation. As shown in Fig. 4, first of all, at a time t1, a signal ERASE END indicated to an end of the erasing operation is set to High level to Low level. Thereby, all of the select transfer signals N1[1] to N1[N] are set to Low level. And the transfer signal N3 remains at High level.

[00082] As a result, the page latch 11 is electrically connected to the cell matrix 2 and separated from the data line 21. Also, the transfer signal 2 slowly changes from at Low level to High level in order to prevent the data from destruction by a charge sharing. This, as shown in Fig. 7b, allows each of the data DATA latched in the latch circuits 19-1 to 19-N to be slowly transferred to the bit lines BL1 to BLN and to be programmed to the memory cells (not shown in Fig. 7a) connected to bit lines BL1 to BLN respectively. Next, at a time t2, the transfer signal N2 is set from High level to Low level. The PROGRAM END signal is set to High level contemporarily and the programming operation is finished.

[00083] Fig. 8a and Fig. 8b show circuit examples of the control circuits to control the transfer signal N2 (hereafter, which are called N2 control circuits). As shown in Fig. 8a and 8b, transfer signals N2 SLOW and N2 QUICK are inputted to the N2 control circuit 100. At the data loading operation, the transfer signal N2 QUICK is set to Low level. Thereby, a output node 102 is sharply charged from a voltage supply VCC via a transistor PMOS 101. On the other hand, at the programming operation or the after-stated page latch reading out operation, the transfer signal N2 SLOW is set to Low level. Thereby, the output node 102 is

slowly charged from the voltage supply VCC via a depletion type NMOS 104 and a PMOS resistor 103 or resistance 105. These allow the transfer signal N2 to be slowly changed from Low level to High level.

[00084] In order to prevent the data from destruction by the charge sharing, an inverter circuit can be located between the latch circuits 19-1 to 19-N and the third transfer gates 17-1 to 17-N, other than the transfer signal N2 being made to change slowly from Low level to High level. But in view of high integration, it is more preferable that the transfer signal N2 is made to change slowly from Low level to High level than that the inverter circuit is located between the latch circuits 19-1 to 19-N and the third transfer gates 17-1 to 17-N.

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[00085] READING OUT OPERATION.

[00086] As shown in Fig. 5, first of all, at a time t1, each of the chip enable signal /CE and the output enable signal /OE are set from High level to Low level, thereby allowing the signal N4 to be set from Low level to High level. Also, the signal N3 remains at High level and the signal N2 remains at Low level.

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[00087] As a result, the page latch 11 is electrically connected to the cell matrix 2 and the data line 21 is electrically connected to the read out circuit 27 (see Fig.2). This allows data DATA stored in the memory cell to be transferred to the connection nodes 23-1 to 23-N via the bit lines BL1 to BLN. After that, when the chip enable signal /CE and the output enable signal /OE are set to Low level respectively, the address signal ADD is inputted to the chip. As a result, by the address signal ADD, one of the N select transfer signals N1[1] to N1[N] is selected typically, and the selected one of the select transfer signals is set from Low level to High level. Thereby, as shown in Fig. 7c, a selected one of the bit lines BL1 to BLN (for example, BL1 in Fig. 7c) is connected to the data line 21 via the connection node 23-1,

and the data DATA stored in the memory cell is transferred to the read out circuit 27, and the data DATA which is transferred to the read out circuit 27 is outputted from the read out circuit 27 as a read out data.

[00088] Next, at a time t2, the chip enable signal /CE and the output enable signal /OE are set from Low level to High level respectively. Thereby the transfer signal N4 is set from High level to Low level, and the reading out operation is over.
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[00089] PAGE LATCH READING OPERATION.

[00090] Fig. 6 shows a waveform diagram which indicates a page latch reading out operation illustrated in Fig. 2. And Fig. 7d shows a state diagram of the page latch 11 at the page latch reading out operation.
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[00091] As shown in Fig. 6, first of all, at a time t1, similar to the reading out operation, the chip enables signal /CE and the output enable signal /OE are set from High level to Low level respectively. Thereby, at the page latch reading out operation, the signal
15 N4 is set from Low level to High level, and the signal N3 is set from High level to Low level.

[00092] As a result, the first transfer gates 13-1 to 13-N turn OFF, the page latch 11 is electrically separated from the cell matrix 2. Also, the fourth transfer gate 25 turns ON. The data line 21 is electrically connected to the read out circuit 27. Furthermore, the signal N2 slowly changes from at Low level to High level. This allows data latched in the latch circuit
20 19-1 to 19-N to be slowly transferred to the connection nodes 23-1 to 23-N. After that, similar to the reading out operation, when the chip enable signal /CE and the output enable signal /OE are set to Low level respectively, the address signal ADD is inputted into the chip. Thereby, by the address signal ADD, one of the N select transfer signals N1[1] to N1[N] is selected typically, and the selected one of the select transfer signals is set from Low level to

High level. As a result, as shown in Fig. 7d, a selected one of the latch circuits 19-1 to 19-N (for example, a latch circuit 19-1 in Fig. 7c) is connected to the data line 21 via the connection node 23-1, and the data DATA latched in the memory cell is transferred to the read out circuit 27, and the data DATA which transferred to the read out circuit 27 is outputted from the read out circuit 27 as a read out data.

[00093] Next, at a time t2, the chip enable signal /CE and the output enable signal /OE are set from Low level to High level respectively. Thereby the transfer signal N3 is set from Low level to High level, and the signal N2 and N4 are set from High level to Low level respectively, then the page latch reading out operation is over.

[00094] Another type of the page latch reading out operation is now described. The page latch reading out operation which is explained with reference to Fig. 6 and Fig. 7 is carried out at the state where the first transfer gates 13-1 to 13-N are set to be OFF and the page latch 11 is electrically separated from the cell matrix 2. However, the page latch reading out operation also may be carried out at a state where the page latch 11 is electrically connected to the cell matrix 2. Hereinafter, another type of the page latch reading out operation is described.

[00095] Fig. 9 shows a waveform diagram of another page latch reading out operation of the page latch 11 illustrated in Fig. 2. Also, Fig. 10a shows a state diagram of the page latch 11 at this another type of the page reading out operation. As shown in Fig. 9 and Fig. 10, this another type of the page latch reading out operation differs from the page latch reading out operation which is explained with reference to Fig. 6 and Fig. 7d, in the viewpoint that the memory cell is set to be non-selected state, while in the latter type of the latch reading out operation the signal N3 remains at High level and the first transfer gates 13-1 to 13-N are ON.

[00096] With the memory cell MC being at non-selected state, even if the first transfer gates 13-1 to 13-N are at ON state, the data stored in the memory cell is not transferred to the bit lines BL1 to BLN. Therefore, the data latched in the latch circuits 19-1 to 19-N can be transferred to the connection nodes 23-1 to 23-N. As described above, in this another type of 5 the page latch reading out operation, the data DATA latched in the latch circuits 19-1 to 19-N can be transferred to the read out circuit 27.

[00097] In order to set the memory cell to be non-selected state, there are some ways in accordance with a type of nonvolatile memory cell, which are grouped into two types whether the nonvolatile memory has a select transistor or not.

[00098] Fig. 10a shows a general NOR type nonvolatile memory cell. The NOR type nonvolatile memory cell does not have a select transistor. In this type of a nonvolatile memory cell, in order to set the memory cell MC to be non-selected, it is necessary to set all of the word lines WL in the cell matrix 2 to be at a non-select voltage which is typically 0 V. Also, Fig. 10b shows a three-transistor type nonvolatile memory. The three-transistor type nonvolatile memory cell has a select transistor STD connected to a bit line and a select transistor STS connected to a source line. In this type of a nonvolatile memory cell, in order to set the memory cell MC to be non-selected, it is necessary to set all the select transistors STD connected to the bit line or all the select transistors STS connected to the source line in the cell matrix 2, to be non-select voltage which is typically 0V.

[00099] With the memory cell MC being at non-selected state, even if the first transfer gates 13-1 to 13-N are ON state, the data stored in the memory cell MC is not transferred to the bit lines BL1 to BLN.

[000100] Next, an example of a control circuit to control the nonvolatile semiconductor memory device of the first embodiment with operations thereof, is now described. Fig. 11

shows a block diagram illustrating one example of the control circuit. Fig. 11 specifically shows a block diagram of a control circuit to control from the data loading operation to the data programming operation.

5 [000101] NORMAL OPERATION.

[000102] Fig. 12 and Fig. 13 show waveform diagrams at normal operation of the control circuit illustrated in Fig. 11 respectively. Fig. 2 and Fig. 3 are originally one waveform diagram, which is divided into two waveform diagrams. Therefore, times t1, t2, , , illustrated in Fig. 12 correspond with times t1, t2, , , illustrated in Fig. 13, respectively.

10 [000103] As shown in Fig. 11, the control circuit 31 includes a data load control logic 33, a finish logic after data load 35, an erase control logic 37, a program control logic 39, a verify control logic 41, a verify result judgment logic 43 and a recovery control logic 45.

15 [000104] The data load control logic 33 receives the chip enable signal /CE and the write enable signal /WE. When both of the chip enable signal /CE and the write enable signal /WE are set to Low level, a READY//BUSY signal is set from High level to Low level (at time t1 in Fig. 12). The READY//BUSY signal is a signal that indicates whether the nonvolatile semiconductor memory device is a ready state or a busy state. When the READY//BUSY signal is at High level, the READY//BUSY signal indicates the ready state. When the READY//BUSY signal is at Low level, the READY//BUSY signal indicates the busy state.

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[000105] The data load control logic 33 outputs DATA LOAD 1 to DATA LOAD N signals when both of the chip enable signal /CE and the write enable signal /WE are set to Low level. Each of the DATA LOAD 1 to DATA LOAD N signals is a signal to control timings of N times of data loading. The DATA LOAD1 to DATA LOADN signals are

typically set from Low level to High level in numerical order (during the time period between t1 and t2 in Fig. 12 (DATA LOAD)). When all of the DATA LOAD1 to DATA LOADN are set from High level to Low level, the data load logic 33 outputs a DATA LOAD END signal which is a signal that indicates an end of the data loading operation and is inputted to the

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finish logic after data load 35.

[000106] The finish logic after data load 35 outputs the ERASE START signal which is at High level when the a DATA LOAD END signal is set to High level and the TEST signal is set to Low level. The TEST signal is set to Low level at the normal operation. The ERASE START signal is inputted to the erase control logic 37.

[000107] The erase control logic 37 outputs an ERASE 1 to ERASE N' signals when the ERASE START signal is set to High level. Each of the ERASE 1 to ERASE N' signals is a signal to control timings of the N' times of data erasing. The ERASE 1 to ERASE N' are typically set from Low level to High level in numerical order (during the time period between t3 and t4 in Fig. 12 (ERASE)). When all of the ERASE 1 to ERASE N' signals are set from High level to Low level, the erase control logic 37 outputs a ERASE END signal which is a signal that indicates an end of the erasing operation and is inputted to an OR logic gate 38.

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[000108] The OR logic gate 38 outputs a PROGRAM START signal which is High level when one of an ERASE END signal and a REPROGRAM START signal is set to High level. The PROGRAM START signal is a signal which indicates a start of the programming operation and is inputted to the program control logic 39.

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[000109] The program control logic 39 outputs PROGRAM 1 to PROGRAM N'' signals when the PROGRAMS START signal is set to High level. Each of the PROGRAM 1 to PROGRAM N'' signals indicates a signal to control timings of N'' times of data programming. The PROGRAM 1 to PROGRAM N'' signals are typically set from Low

level to High level in numerical order (during the time period between t5 and t6 in Fig. 12 (PROGRAM)). When all of the PROGRAM 1 to PROGRAM N'' signals are set from High level to Low level, the program control logic 39 outputs a PROGRAM END signal which is a signal that indicates an end of the programming operation and is inputted to a verify control logic 41.

[000110] When the PROGRAM END signal is set to Low level, the verify control logic 41 outputs VERIFY 1 to VERIFY N''' signals. Each of the VERIFY 1 to VERIFY N''' signals indicates a signal to control timings of N''' times of verifying. The VERIFY 1 to VERIFY N''' signals are typically set from Low level to High level in numerical order (during the time period between t7 and t8 in Fig. 13 (VERIFY)). When all of the VERIFY 1 to VERIFY N''' signals are set from High level to Low level, the verify control logic 41 outputs a VERIFY END (I) signal which is a signal that indicates an end of the verifying operation and is inputted to a verify result judgment logic 43.

[000111] When both of the VERIFY END (I) signal and a VERIFY PASS signal are set to High level, the verify result judgment logic 43 outputs the VERIFY END (I) of High level. When the VERIFY PASS signal is set to Low level, the verify result judgment logic 43 outputs the PROGRAM START signal of Low level. The PROGRAM START signal indicates a start of a reprogramming operation and is inputted to the OR logic gate 38. When a REPROGRAM START signal is set to High level, the reprogramming operation, which is shown as REPROGRAM in Fig. 12, is carried out. Also, the VERIFY END (II) signal is a signal which indicates an end of the verifying operation at an normal operation and is inputted to the OR logic gate 44.

[000112] The OR logic gate 44 outputs a RECOVERY START (I) signal of High level, when one of the VERIFY END (II) signal and the RECOVERY START (II) signal is set to

High level. The RECOVERY START (I) signal is a signal which indicates a start of a recovery operation and is inputted to a recovery control logic 45.

[000113] When the RECOVERY START (I) signal is set to High level, the recovery control logic 45 outputs RECOVRY 1 to RECOVRY N^{'''} signals. Each of the RECOVRY 1 to RECOVRY N^{'''} signals indicates a signal to control timings of N^{'''} times of recovery. The RECOVRY 1 to RECOVRY N^{'''} signals are typically set from Low level to High level in numerical order (during the time period between t9 and t10 in Fig. 13 (RECOVEY). When all of the RECOVRY 1 to RECOVRY N^{'''} signals are set from High level to Low level, the recovery control logic 45 outputs a RECOVERY END signal which is a signal that indicates an end of the recovery operation. When the RECOVERY END signal is set from High level to Low level, a READY//BUSY signal is set from Low level to High level. As a result, the semiconductor memory device becomes in a halted condition (at a time t11 in Fig. 13).

[000114] As stated above, the control circuit 31 makes the semiconductor memory device to carry out the data loading operation, the data erasing operation, the data programming operation and the verifying operation automatically at the normal operation. And after the verifying operation, the semiconductor memory device carries out the recovery operation, then is halted. The verifying operation can be omitted. In this case, after automatically carrying out the data loading operation, the data erasing operation and the data programming operation, the semiconductor memory device carries out the recovery operation and then, becomes in a halted condition.

[000115] TESTING OPERATION.

[000116] Fig. 14 shows waveform diagram, which indicates a testing operation of the control circuit 31, illustrated in Fig. 11. A time period between a time t1 and a time t2 in

Fig. 14 indicates a period of a data loading operation. Similar to the normal operation, after the data loading operation, the DATA END signal is set to High level. The logic after data load 35 outputs the RECOVERY START (II) of High level, when the DATA LOAD END signal and a TEST signal are set to High level. The TEST signal is set to High level during the testing operation. The RECOVRY START (II) signal is inputted to the OR logic gate 44. Also, the ERASE START signal remains at Low level.

[000117] The OR logic gate 44 outputs a RECOVERY START (I) signal of High level, when one of the VERIFY END (II) signal and the RECOVERY START (II) signal is set to High level. The RECOVERY START (I) signal is inputted to a recovery control logic 45. A recovery period between a time t3 and a time t4 in Fig. 14 is a time period while the recovery operation carried out similar to the normal operation. After the recovery operation is ended, the RECOVERY END signal is set to High level then is set to Low level (RECOVERY END). The READY//BUSY signal is set from Low level to High level, and the semiconductor memory device becomes in a halted condition (at a time t5 in Fig. 14).

[000118] As stated above, at the testing operation, the control circuit 31 carries out the recovery operation after the data loading operation is ended, and makes the semiconductor memory device become in a halted condition.

[000119] A specific circuit schematic of the control circuit 31 is not limited to a circuit schematic illustrated in Fig. 11, and any other circuit configurations including a sequence as to be illustrated in Fig. 15 may be used thereto.

[000120] SECOND EMBODIMENT.

[000121] Fig. 16a and Fig. 16b show data flow diagrams at the data loading operation and the page latch reading out operation of a semiconductor memory device of the second

embodiment respectively. The semiconductor memory device of the second embodiment differs from the semiconductor memory device of the first embodiment in that an error correction system is provided.

[000122] First of all, the error correction system produces an inspection bits from an original data. The inspection bits are produced by an inspection bit generating circuit 51. The inspection bits and the original data are programmed to the corresponding memory cells at the same time. Also, at the reading out operation, the original data and the inspection bits are read out from the memory cells at the same time to judge whether there is an error or not. Data that was judged as an error is corrected and outputted. The judgment of whether there is an error or not, and the error correction if any are carried out at the error correction circuit 53.

[000123] When a test and an inspection of the error correction system are carried out, it is necessary that many suspected error correction patterns are inputted to confirm that the error patterns are corrected regularly. Conventionally, it has taken a long time to test and inspect data by the error correction system because the data are programmed to memory calls after data loading. Nevertheless, in the second embodiment of the present invention, as shown in Fig. 16a and Fig. 16b, at a testing operation, after the data loading operation is carried out, an operation of the semiconductor memory device is once stopped. After that, the page latch operation is carried out. This sequence is the same as the operations of the first embodiment.

[000124] As a result, the data programming operation to the memory cells can be omitted at the test and inspection operation by the error correction system where it is necessary that many suspected error patterns are inputted. Therefore, in the second embodiment, a time for estimating and testing by the inspection bits generating circuit 51 and

the error correction circuit 53 can be shorter than the conventional semiconductor memory device.

[000125] Fig. 17a to Fig. 17c show data flows of the second embodiment of the nonvolatile semiconductor memory device at the normal operation. As shown in Fig. 17a to 5 Fig. 17c, the semiconductor memory device in the second embodiment operates similar to the conventional semiconductor memory device at the normal operation.

[000126] Exemplary applications employing the above-described semiconductor memory device are now described.

[000127] A memory card having the above mentioned semiconductor memory device is 10 shown in Fig. 19. As shown in Fig. 19, the semiconductor memory device receives/outputs predetermined signals and data from/to an external device (not shown).

[000128] A signal line (DAT), a command line enable signal line (CLE), an address line enable signal line (ALE) and ready/busy signal line (R/B) are connected to the memory card having the above mentioned semiconductor memory device. The signal line (DAT) transfers 15 data, address or command signal. The command line enable signal line (CLE) transfers a signal which indicates that a command signal is transferred on the signal line (DAT). The address line enable signal line (ALE) transfers a signal which indicates that an address signal is transferred on the signal line (DAT). The ready/busy signal line (R/B) transfers a signal which indicates whether the memory device is ready or not.

[000129] Another example of a memory card is shown in Fig. 20. The memory card 20 shown in Fig. 20 differs from the memory card presented in Fig. 19 in that the memory card includes a controller which controls the semiconductor memory device and receives/transfers predetermined signals from/to an external device (not shown).

[000130] The controller includes a interface unit (I/F), a micro processor unit (MPU), a buffer RAM and an error correction code unit (ECC). The interface unit (I/F) receives/outputs predetermined signals from/to an external device (not shown). The micro processor unit converts a logical address into a physical address. The buffer RAM stores temporarily data.

5 The error correction code unit generates an error code. And a command signal line (CMD), a clock signal line (CLK) and a signal line (DAT) are connected to the memory card.

[000131] Although memory cards have been described as above, the number of control signal lines, the bit width of the signal line (DAT) and the circuit construction of the controller may be modified while remaining within the scope of the invention.

10 [000132] Another application is shown in Fig. 21. A memory card holder to which the memory card is inserted is shown in Fig. 21. And the card holder is connected to electronic device (not shown). The card holder may have a part of the function of the controller.

15 [000133] Still another application is shown in Fig. 22. As shown in Fig. 22, the memory card or the card holder to which the memory card is inserted, is inserted to a connecting apparatus. The connecting apparatus is connected to a board via a connecting wire and an interface circuit. The board has a CPU (Central Processing Unit) and a bus.

20 [000134] Yet another application is shown in Fig. 23. As shown in Fig. 23, the memory card or the card holder into which the memory card is inserted, is inserted to a connecting apparatus. The connecting apparatus is connected to PC (Personal Computer) via connecting wire.

[000135] As explained above, with the present invention, it is possible to provide a semiconductor memory device that is capable of being easy to specify a cause of an error for the case where a reprogrammed data is an error and operating tests of a page latch and a read out circuit at short time.

[000136] Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

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